		Application/Control No. 09/769,004	Applicant(s)/Patent Under Reexamination SMITH, DAVID	
Notice of References Cited		Examiner Baoquoc N. To	Art Unit 2162	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wall et al. Generatign verifiable microprosessrs state machine code with HDL Design Tools, Industrial Electronics society, Vol. 3, page 2441-2446, Nov 2-6 2003.
	V	Pflanz et al. On-line detection and correction in storage elements with cross-parity check, On-line Testing Workshop, pages 1-5, July 8-10 2002.
	W	Vanbekbergen et al. A design and validation system for asynchronous circuits, Annual ACM IEEE Automation Conference, page 725-730, 1995.□□
	X	Ahdoot et al. IBM FSD VLSI chip desgin methodogy, Annual ACM IEEE Desgin Automation Conference, pages 39-45, 1983.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Pandey et al. Formal verification of PowerPC arrays using symbolic trajectory evaluation, Annual ACM IEEE Desgin Confrence, page 649-654, 1996.
	V	Donald J. McGinnis Autocheck program, program to check vlidity of printed circuit cards and circuit, ACM/CSC-ER, Proceeding of the ACM annual confernce, Vol. 1, page 398-420, year2 1972.
	W	Kern et al. Formal verification in hardware desgin: a survey, ACM Transactions on Design Automation of Electronic System (TODAES), Vol. 4, Issue 2, pages 123-193, 1999.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.